REMARKS

Allowable Subject Matter

Claims 2 and 17 have been objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Applicants have cancelled claim 2 and rewritten it as new claim 21 incorporating the limitations of former claim 1, which is the base claim for original claim 2. Newly presented claims 22-24 are also presented and depend on new claim 21 incorporating all the limitations thereof. Newly presented claims 22-24 include the subject matter of original dependent claims 3-5.

Claim 16 has been amended to incorporate the limitations of claim 17. Claim 17 has been cancelled. Claims 18-20 now depend on currently amended claim 16 and incorporate all the limitations thereof.

Accordingly, it is respectfully submitted that pending claims 16, 18-20, and 21-24 are in condition for allowance and such favorable action is hereby solicited.

Claim Rejections - 35 USC §112

Claims 7-10 have been rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 7 has been rejected on the basis that it recites the limitation "the sidewall spacer" in line 1. The Examiner stated there was insufficient antecedent basis for this limitation in the claim.

Claim 10 has been rejected on the basis that it recites the limitation "the ultra-uniform silicide" in line 2. The Examiner stated there was insufficient antecedent basis for this limitation in the claim.

In reference to claims 7-10, claims 7-10 have been amended to correct a typographical error. Claims 7-10 now depend on claim 6 rather than claim 1 as originally presented.

In reference to claim 7, claim 7 has been amended to depend from claim 6 by correcting the typographical error referring to claim 1. There is now proper antecedent basis for the limitation "the sidewall spacer" in claim 6 upon which claim 7 depends.

In reference to claim 10, claim 10 has been amended to delete the term "ultra-uniform" and to correct the typographical error so claim 10 now depends on claim 6 rather than claim 1. There is now proper antecedent basis for the limitation "silicide" in claim 6 upon which claim 10 depends.

Claims 7-10 now depend from claim 6 and are believed to have proper antecedent bases for the limitations set forth therein. Accordingly, Applicants believe the rejection under 35 U.S.C. has been overcome and the rejection should be withdrawn. Such action is hereby solicited.

Claim Rejections - 35 USC §102

Claims 1, 3, 5, 11, 13, and 15 have been rejected under 35 U.S.C. 102(e) as being anticipated by Iinuma (USPN 6,770,942 B2, hereinafter "Iinuma reference").

Applicants respectfully traverse this rejection since the Applicants' claimed combination, as exemplified in currently amended claims 1 and 11, include the limitation not disclosed in the Iinuma reference of forming trenches in the semiconductor substrate at the outer edges of an insulating sidewall spacer around the gate. The independent claims 1 and 11 have now been amended to clarify the invention and not for reasons related to patentability. The previously claimed combination, as exemplified in claims 1 and 11, has been amended to set forth more clearly that the sidewall spacer is an insulating sidewall spacer and that the trenches are formed in the source/drain junctions in the semiconductor substrate at the outer edge of the insulating sidewall spacer. Support for the amendments is in Applicants' specification, page 5, lines 29-30 and page 8, lines 25-28.

The Iinuma reference discloses a semiconductor device including an element separating insulating film to separate an element region. A silicide film over the source drain regions extends onto the element separating insulating film. A contact hole extends through an interlayer insulating film, the element separating film, and reaches the silicide film. The contact hole includes a trench portion whose one end contacts the edge of the silicide film in

the bottom of the contact hole and in an upper portion of the element separating insulating film. The trench in the Iinuma reference is formed in the element separating insulating film in the bottom of the contact holes and not at the outer edge of an insulating sidewall spacer as claimed by Applicants.

Additionally, the Iinuma reference specifically discloses that it is possible to prevent the trench portion from contacting the first diffusion region, or source drain region (see col.7, l. 48-50). It is clear from Applicants' disclosure that the trenches in the present invention do contact the sour/drain regions; therefore, at least to this extent the Iinuma reference teaches away from Applicants' invention.

Furthermore, the Iinuma reference does not disclose or suggest the problem solved by Applicants' invention, i.e. reducing lateral silicide growth into the channel of the transistor, much less solve it. The Iinuma reference is directed to an entirely different problem of formation of an abnormally grown silicide film at the outer edges of the source/drain regions (see col. 7, l. 52-53 and FIG. 13, element 142).

In reference to claims 1 and 11, from the above, it is evident that the Iinuma reference lacks forming trenches around the gate at the outer edges of an insulating spacer as exemplified in currently amended claims 1 and 11. In light of the foregoing, Applicants submit that claims 1 and 11, as amended, are patentable over the Iinuma reference.

Claim 3 depends from claim 1 and includes all the limitations set forth therein. Accordingly, claim 3 is patentable over the Iinuma reference for the reasons set forth above with respect to claim 1. Additionally, claim 3 adds the element of forming the trenches uses an etching process that etches the semiconductor substrate. Applicants submit that claim 3 is patentable over the Iinuma reference.

Claim 11 is directed to an integrated circuit including trenches in the semiconductor substrate around the gate. For the reasons set forth above, Applicants respectfully submit that the Iinuma reference fails to disclose or suggest the structure claimed in claim 11, and

specifically fails to disclose or suggest trenches around the outer edges of an insulating spacer around the gate. Applicants submit that claim 11 is patentable over the Iinuma reference.

With regard to claim 13, the Examiner has stated that the Iinuma reference discloses that the trenches extend into the semiconductor substrate (1) to a level lower than the silicide (14b). Applicants traverse this rejection.

Claim 13 depends on claim 11 and includes all the limitations set forth therein. Accordingly, claim 13 is patentable for the reasons set forth with respect to claim 11.

Additionally, there is no disclosure or suggestion by the Iinuma reference with respect to the depth of the trenches. Applicants submit that the Iinuma reference is silent in this regard, and at most, the drawings in the Iinuma reference show the trenches arguably extending to the lower level of the silicide layer, but not to a level lower than the silicide layer as claimed in claim 13. Applicants submit that claim 13 is patentable over the Iinuma reference.

In reference to claim 5, Applicants' traverse this rejection. Claim 5 depends on claim 1 and includes all the limitations set forth therein. Accordingly, claim 5 is patentable for the reasons set forth with respect to claim 1. Applicants submit that claim 5 is patentable over the Iinuma reference.

Similarly, in reference to claim 15, claim 15 depends on claim 11 and includes all the limitations set forth therein. Accordingly, claim 15 is patentable for the reasons set forth above with respect to claim 11. Applicants submit that claim 15 is patentable over the Iinuma reference.

It is respectfully submitted that the now amended independent claims 1 and 11, and the respective claims 3, 5 and 13, 15 depending therefrom, are no longer anticipated by the Iinuma reference under 35 USC §102.

Claim Rejections - 35 USC §103

Claims 1, 3, 11, and 12 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Kang et al. (USPN 5,665,990, hereinafter "Kang reference") in view of Merrill (USPN 5,918,141, hereinafter "Merrill reference").

Applicants respectfully traverse these rejections.

In reference to currently amended claim 1, Kang discloses a metal oxide semiconductor device in which a sidewall spacer is removed to form a groove structure in the substrate adjacent the gate. A polysilicon layer is formed on the groove structure to form a second gate electrode at both sides of the gate. There is no insulating sidewall spacer around the gate in the Kang reference as claimed by Applicants. The "sidewall spacer" referred to by the Examiner in the Kang reference is a second gate electrode (see col. 2, lines 53-54), not an "insulating sidewall spacer" as claimed by Applicants.

The Examiner has stated:

> Kang does not disclose the use of a silicide with the source/drain junctions ...

Applicants agree and submit that the Kang reference therefore cannot, and does not, recognize or address the problem solved by Applicants' invention. Since there is no silicide disclosed or suggested in the Kang reference, there can be no suggestion that the structure or method disclosed in the Kang reference recognizes or addresses reducing lateral silicide growth toward the channel of the transistor.

With respect to Merrill, the Examiner has stated:

> Merrill (USPN 5,918,141) illustrates a device which uses a silicide layer with the source/drain junctions and the gate in figures 1A-1E. Furthermore Merrill discloses that using a silicide reduces contact resistance which leads to the benefit of a high speed device (column 1, lines 15-27). In view of Merrill, it would therefore be obvious to use silicide with the source/drain junctions and gate in the device of Kang.

Applicants submit that the Merrill reference does not disclose or suggest the problem of reducing lateral silicide growth.

The Merrill reference is directed to a semiconductor device using a silicide to reduce contact resistance. The Merrill reference does not disclose or suggest the problem of lateral silicide growth or a proposed solution.

Since both the Kang reference and the Merrill reference taken as a whole are silent with respect to the problem solved by Applicants' invention, it is respectfully submitted that there is no teaching or suggestion to combine the references to arrive at Applicants' invention as required by 35 USC §103.

Even if combined, however, the combination of the Kang reference and the Merrill reference fails to disclose or suggest the Applicants' claimed invention. The Kang reference and the Merrill reference, taken either singly, or in combination, fail to disclose or suggest forming trenches at the outer edges of an insulating spacer around the gate of a transistor.

Accordingly, it is submitted that Claim 1 as currently amended is patentable over the Kang reference in view of the Merrill reference.

In reference to claim 3, claim 3 depends on claim 1 and includes all the limitations thereof. Accordingly, claim 3 is patentable for the reasons set forth with respect to claim 1.

In reference to claim 11, the Kang reference discloses a metal oxide semiconductor device in which an insulating sidewall spacer is removed to form a groove structure in the substrate adjacent the gate. A polysilicon layer is formed on the groove structure to form a second gate electrode at both sides of the gate (see col. 2, lines 48-56). There is no insulating sidewall spacer around the gate in the Kang reference as claimed by Applicants. The "sidewall spacer" referred to by the Examiner in the Kang reference is a second gate electrode not an "insulating sidewall spacer" as claimed by Applicants.

The Examiner has stated:

> Kang does not disclose the use of a silicide with the source/drain junctions ...

Applicants agree and submit that the Kang reference therefore cannot, and does not, recognize or address the problem solved by Applicants' invention. Since there is no silicide taught or suggested in the Kang reference, there can be no suggestion that the structure or method disclosed in the Kang reference recognizes or addresses reducing lateral silicide growth toward the channel of the transistor.

With respect to the Merrill reference, the Examiner has stated:

> Merrill (USPN 5,918,141) illustrates a device which uses a silicide layer with the source/drain junctions and the gate in figures 1A-1E. Furthermore Merrill discloses that using a silicide reduces contact resistance which leads to the benefit of a high speed device (column 1, lines 15-27). In view of Merrill, it would therefore be obvious to use silicide with the source/drain junctions and gate in the device of Kang.

Applicants submit that the Merrill reference does not teach or suggest the problem of reducing lateral silicide growth.

Since both the Kang reference and the Merrill reference taken as a whole are silent with respect to the problem solved by Applicants' invention, it is respectfully submitted that there is no teaching or suggestion to combine the references to arrive at Applicants' invention as required by 35 USC §103.

Even if combined, however, the combination of the Kang reference and the Merrill reference fails to disclose or suggest the Applicants' claimed invention. The Kang reference and the Merrill reference, taken either singly or in combination, fail to teach or suggest forming trenches at the outer edges of an insulating spacer around the gate of a transistor.

Accordingly, it is submitted that Claim11 as currently amended is patentable over the Kang reference in view of the Merrill reference.

In reference to claim 12, the Examiner has stated:

> With regard to claim 12, there is a sidewall spacer (8) around the gate (4) wherein the trenches are at the outer edge of the sidewall spacer (8).

Applicants traverse this rejection. Claim 12 has been cancelled, but the limitations set forth therein have been incorporated into currently amended claim 11.

The Kang reference, as previously discussed, forms a second gate electrode (8) which is semiconductive and, therefore, not an insulating sidewall spacer around the gate as claimed by Applicants. Although the Kang reference refers to the second gate electrode as a "sidewall spacer," it is clear that the "sidewall spacer" in the Kang reference is a polysilicon layer (col. 2, lines 53-54) that is not an insulating sidewall spacer as claimed by Applicants. Furthermore, the trenches in the Kang reference are below the second gate electrode and not at the outer edge of the second gate electrode. The "sidewall spacer" in the Kang reference

fills the trenches and is not at the outer edges of an insulating sidewall spacer around the gate as claimed by Applicants.

Applicants submit that claim 11 is patentable over the combination of the Kang reference in view of the Merrill reference under 35 U.S.C. 103.

Claim 4 has been rejected under 35 U.S.C. 103(a) as being unpatentable over the Kang reference in view of the Merrill reference as applied to claim 1 and further in view of Russell et al. (USPN 5,648,175, hereinafter "Russell reference").

In reference to claim 4, claim 4 depends on claim 1 and includes all the limitations thereof. Accordingly, claim 4 is patentable for the reasons set forth above with respect to claim 1.

Additionally, the Russell reference does not teach or suggest the problem solved by Applicants' invention. The Russell reference discloses a method and apparatus for providing a dielectric layer having a low dielectric constant. Applicants submit that the Russell reference does not teach or suggest the problem of reducing lateral silicide growth.

Since the Kang reference, the Merrill reference, and the Russell reference taken as a whole are silent with respect to the problem solved by Applicants' invention, it is respectfully submitted that there is no teaching or suggestion to combine the references as a whole to arrive at Applicants' invention as required by 35 USC §103.

Even if combined, however, the combination of the Kang reference, the Merrill reference, and the Russell reference fails to teach or suggest the Applicants' claimed invention. The Kang reference, the Merrill reference, and the Russell reference taken singly, or in combination, fail to disclose or suggest forming trenches at the outer edges of an insulating spacer around the gate of a transistor.

Accordingly, it is submitted that Claim 4 as currently amended is patentable over the Kang reference in view of the Merrill reference in further view of the Russell reference taken singly, or in combination.

Claim 4 also has been rejected under 35 U.S.C. 103(a) as being unpatentable over the Kang reference in view of the Merrill reference as applied to claim 1 and further in view of Sekiguchi (USPN 6,333,255 B1, hereinafter "Sekiguchi reference").

In reference to claim 4, claim 4 depends on claim 1 and includes all the limitations thereof. Accordingly, claim 4 is patentable for the reasons set forth above with respect to claim 1.

Additionally, the Sekiguchi reference is directed to a semiconductor device having a "gas-dielectric interconnect structure" and does not teach or suggest the problem solved by Applicants invention. Since the Kang reference, the Merrill reference, and the Sekiguchi reference taken as a whole do not teach or suggest the problem solved by Applicants' invention, it is respectfully submitted that there is no teaching or suggestion to combine the references to arrive at Applicants' invention as required by 35 USC §103.

Even if combined, however, the combination of the Kang reference, the Merrill reference, and the Sekiguchi reference fails to disclose or suggest the Applicants' claimed invention. The Kang reference, the Merrill reference, and the Sekiguchi reference taken singly, or in combination, fail to teach or suggest forming trenches at the outer edges of an insulating spacer around the gate of a transistor.

Accordingly, it is submitted that Claim 4 is patentable over the Kang reference in view of the Merrill reference in further view of the Sekiguchi reference taken singly, or in combination.

Claim 5 has been rejected under 35 U.S.C. 103(a) as being unpatentable over the Kang reference in view of the Merrill reference as applied to claim 1 above and further in view of Liauh (USPN 5,027,185, hereinafter "Liauh reference") and further in view of Wald et al. (USPN 5,932,491, hereinafter "Wald reference").

Applicants traverse this rejection.

Claim 5 depends on currently amended claim 1 and includes all the limitations thereof. Accordingly, claim 5 is patentable for the reasons set forth with regard to claim 1.

In reference to claim 5, the Kang reference teaches a metal oxide semiconductor device in which an insulating sidewall spacer is removed to form a groove structure in the substrate adjacent the gate. A polysilicon layer is formed on the groove structure to form a second gate electrode at both sides of the gate (see col. 2, lines 48-56). There is no insulating sidewall spacer around the gate in the Kang reference as claimed by Applicants. The "sidewall spacer" referred to by the Examiner in the Kang reference is a second gate electrode (see col. 2, lines 53-54) not an "insulating sidewall spacer" as claimed by Applicant.

The Examiner has stated:

> Kang does not disclose the use of a silicide with the source/drain junctions ...

Applicants agree and submit that the Kang reference therefore cannot, and does not, teach or suggest the problem solved by Applicants' invention. Since there is no silicide taught or suggested in the Kang reference, there can be no suggestion that the structure or method taught in the Kang reference recognizes or addresses reducing lateral silicide growth toward the channel of the transistor.

The Examiner also has stated:

> Kang does not disclose the exact material which is used for the contact.

Applicants agree that the Kang reference does not disclose the materials used for contacts as claimed by Applicants.

The Merrill reference is directed to a semiconductor device using a silicide to reduce contact resistance. The Merrill reference does not teach or suggest the problem of lateral silicide growth or a proposed solution.

Since both the Kang reference and the Merrill reference taken as a whole are silent with respect to the problem solved by Applicants' invention, it is respectfully submitted that there is no teaching or suggestion to combine the references to arrive at Applicants' invention as required by 35 USC §103.

Even if combined, however, the combination of the Kang reference and the Merrill reference fails to teach or suggest the Applicants' claimed invention. The Kang reference and the Merrill reference, taken either singly, or in combination, fail to teach or suggest forming trenches at the outer edges of an insulating spacer around the gate of a transistor. The Kang

reference and the Merrill reference, taken either singly, or in combination, also fail to teach or suggest the contact materials claimed by Applicants.

The Liauh reference is directed to a process for forming a polycide gate structure including a metal salicide to reduce sheet resistance of the gate, and having metal silicides formed in the source and drain regions to minimize sheet resistance. The Liauh reference does not teach the problem of lateral silicide growth or any proposed solution.

Similarly, the Wald reference does not teach the problem of lateral silicide growth or any proposed solution.

Since the Kang reference, the Merrill reference, the Liauh reference, and the Wald reference taken as a whole are silent with respect to the problem solved by Applicants' invention, it is respectfully submitted that there is no teaching or suggestion to combine these references to arrive at Applicants' invention as required by 35 USC §103.

Even if combined, however, the combination of the proposed combination of the Kang reference, the Merrill reference, the Liauh reference, and the Wald reference fails to teach or suggest the Applicants' claimed invention. These references, taken either singly, or in combination, fail to teach or suggest forming trenches at the outer edges of an insulating spacer around the gate of a transistor.

Accordingly, it is submitted that Claim 5 as currently amended is patentable over the Kang reference, the Merrill reference, the Liauh reference, and the Wald reference taken singly, or in combination.

Claim 5 has been rejected under 35 U.S.C. 103(a) as being unpatentable over the Kang reference in view of the Merrill reference as applied to claim 1 above and further in view of the Liauh reference and further in view of Yoshida et al. (USPN 6,580,143 B2, hereinafter "Yoshida reference").

Claim 5 depends on currently amended claim 1 and includes all the limitations thereof. Accordingly, claim 5 is patentable for the reasons set forth with regard to claim 1.

In reference to claim 5, the Kang reference teaches a metal oxide semiconductor device in which an insulating sidewall spacer is removed to form a groove structure in the

substrate adjacent the gate. A polysilicon layer is formed on the groove structure to form a second gate electrode at both sides of the gate (see col. 2, lines 48-56). There is no insulating sidewall spacer around the gate in the Kang reference as claimed by Applicants. The "sidewall spacer" referred to by the Examiner in the Kang reference is a second gate electrode not an "insulating sidewall spacer" as claimed by Applicant.

The Examiner has stated:

> Kang does not disclose the use of a silicide with the source/drain junctions ...

Applicants agree and submit that the Kang reference therefore cannot, and does not, recognize or address the problem solved by Applicants' invention. Since there is no silicide taught or suggested in the Kang reference, there can be no suggestion that the structure or method disclosed in the Kang reference recognizes or addresses reducing lateral silicide growth toward the channel of the transistor.

The Examiner also has stated:

> Kang does not disclose the exact material which is used for the contact.

Applicants agree that the Kang reference does not disclose the materials used for contacts as claimed by Applicants.

The Merrill reference is directed to a semiconductor device using a silicide to reduce contact resistance. The Merrill reference does not teach or suggest the problem of lateral silicide growth or a proposed solution.

Since both the Kang reference and the Merrill reference taken as a whole are silent with respect to the problem solved by Applicants' invention, it is respectfully submitted that there is no teaching or suggestion to combine the references to arrive at Applicants' invention as required by 35 USC §103.

Even if combined, however, the combination of the Kang reference and the Merrill reference fails to teach or suggest the Applicants' claimed invention. The Kang reference and the Merrill reference, taken either singly, or in combination, fail to teach or suggest forming trenches at the outer edges of an insulating spacer around the gate of a transistor. The Kang reference and the Merrill reference, taken either singly, or in combination, also fail to teach or suggest the contact materials claimed by Applicants.

The Liauh reference is directed to a process for forming a polycide gate structure including a metal salicide to reduce sheet resistance of the gate, and having metal silicides formed in the source and drain regions to minimize sheet resistance. The Liauh reference does not teach the problem of lateral silicide growth or any proposed solution.

Similarly, the Yoshida reference does not teach the problem of lateral silicide growth or any proposed solution. The Yoshida reference is directed to a thin-film circuit substrate having an organic insulating film with a surface modification layer.

Since the Kang reference, the Merrill reference, the Liauh reference, and the Yoshida reference taken as a whole are silent with respect to the problem solved by Applicants' invention, it is respectfully submitted that there is no teaching or suggestion to combine these references to arrive at Applicants' invention as required by 35 USC §103.

Even if combined, however, the proposed combination of the Kang reference, the Merrill reference, the Liauh reference, and the Yoshida reference fails to teach or suggest the Applicants' claimed invention. These references, taken either singly, or in combination, fail to teach or suggest forming trenches at the outer edges of an insulating spacer around the gate of a transistor.

Accordingly, it is submitted that Claim 5 as currently amended is patentable over the Kang reference, the Merrill reference, the Liauh reference, and the Yoshida reference taken singly, or in combination.

Claims 6, 8, 16, and 18 have been rejected under 35 U.S.C. 103(a) as being unpatentable over the Kang reference in view of the Merrill reference.

Applicants traverse these rejections.

In reference to claim 6, the Kang reference teaches a metal oxide semiconductor device in which an insulating sidewall spacer is removed to form a groove structure in the substrate adjacent the gate. A polysilicon layer is formed on the groove structure to form a second gate electrode at both sides of the gate (see col. 2, lines 48-56). There is no insulating sidewall spacer around the gate in the Kang reference as claimed by Applicants. The

"sidewall spacer" referred to by the Examiner in the Kang reference is a second gate electrode not an "insulating sidewall spacer" as claimed by Applicant.

The Examiner has stated:

> Kang does not disclose the use of a silicide with the source/drain junctions ...

Applicants agree and submit that the Kang reference therefore cannot, and does not, recognize or address the problem solved by Applicants' invention. Since there is no silicide taught or suggested in the Kang reference, there can be no suggestion that the structure or method disclosed in the Kang reference recognizes or addresses reducing lateral silicide growth toward the channel of the transistor.

With respect to the Merrill reference, the Examiner has stated:

> Merrill (USPN 5,918,141) illustrates a device which uses a silicide layer with the source/drain junctions and the gate in figures 1A-1E. Furthermore Merrill discloses that using a silicide reduces contact resistance which leads to the benefit of a high speed device (column 1, lines 15-27). In view of Merrill, it would therefore be obvious to use silicide with the source/drain junctions and gate in the device of Kang.

Applicants submit that the Merrill reference does not disclose or suggest the problem of reducing lateral silicide growth.

Since both the Kang reference and the Merrill reference taken as a whole are silent with respect to the problem solved by Applicants' invention, it is respectfully submitted that there is no teaching or suggestion to combine the references to arrive at Applicants' invention as required by 35 USC §103.

Even if combined, however, the combination of the Kang reference and the Merrill reference fails to teach or suggest the Applicants' claimed invention. The Kang reference and the Merrill reference, taken either singly, or in combination, fail to teach or suggest forming trenches at the outer edges of an insulating spacer around the gate of a transistor.

Accordingly, it is submitted that Claim 6 as currently amended is patentable over the Kang reference in view of the Merrill reference.

In reference to claim 8, claim 8 depends on claim 6 as currently amended and includes all the limitations thereof. Accordingly, claim 8 is patentable for the reasons set forth above with respect to claim 6.

In reference to claim 16 as currently amended, the Examiner has stated:

> With regard to claim 16, there is a sidewall spacer (8) around the gate (4) wherein the trenches are at the outer edge of the sidewall spacer (8).

The Kang reference as previously discussed forms a second gate electrode (8) which is semiconductive around the gate, and specifically does not disclose an insulating liner around the gate, an insulating film over the insulating liner, and trenches in the semiconductor substrate at the outer edges of the insulating film as claimed in claim 16.

Although the Kang reference refers to the second gate electrode as a "sidewall spacer," it is clear that the "sidewall spacer" in the Kang reference is a polysilicon layer (col. 2, lines 53-54) that is not an insulating sidewall spacer as claimed by Applicants. Furthermore, the trenches in the Kang reference are below the second gate electrode and not at the outer edge of the second gate electrode disclosed in the Kang reference. The "sidewall spacer" in the Kang reference fills the trenches and is not at the outer edges of an insulating film around the gate as claimed by Applicants.

The Examiner has stated:

> Kang does not disclose the use of a silicide with the source/drain junctions ...

Applicants agree and submit that the Kang reference therefore cannot, and does not, recognize or address the problem solved by Applicants' invention. Since there is no silicide disclosed or suggested in the Kang reference, there can be no suggestion that the structure or method disclosed in the Kang reference recognizes or addresses reducing lateral silicide growth toward the channel of the transistor.

With respect to the Merrill reference, the Examiner has stated:

> Merrill (USPN 5,918,141) illustrates a device which uses a silicide layer with the source/drain junctions and the gate in figures 1A-1E. Furthermore Merrill discloses that using a silicide reduces contact resistance which leads to the benefit of a high speed device (column 1, lines 15-27). In

view of Merrill, it would therefore be obvious to use silicide with the source/drain junctions and gate in the device of Kang.

Applicants submit that the Merrill reference does not disclose or suggest the problem of reducing lateral silicide growth.

Since both the Kang reference and the Merrill reference taken as a whole do not teach or suggest the problem solved by Applicants' invention, it is respectfully submitted that there is no teaching or suggestion to combine the references to arrive at Applicants' invention as required by 35 USC §103.

Even if combined, however, the combination of the Kang reference and the Merrill reference fails to teach or suggest the Applicants' claimed invention. The Kang reference and the Merrill reference, taken either singly, or in combination, fail to teach or suggest an integrated circuit including an insulating liner around the gate, an insulating film over the insulating liner, and trenches in the semiconductor substrate at the outer edges of the insulating film.

Accordingly, it is submitted that Claim 16 as currently amended is patentable over the Kang reference in view of the Merrill reference taken either singly, or in combination.

In reference to claim 18, claim 18 depends on claim 16 and includes all the limitations thereof. Accordingly, claim 18 is patentable for the reasons set forth with respect to claim 16.

Claim 9 has been rejected under 35 U.S.C. 103(a) as being unpatentable over the Kang reference in view of the Merrill reference as applied to claim 6 above and further in view of the Russell reference.

Applicants traverse this rejection. Claim 9 depends on claim 6 and includes all the limitations thereof. Accordingly, claim 9 is patentable for the reasons set forth above with respect to claim 6.

Additionally, the Russell reference does not teach or suggest the problem solved by Applicants' invention. The Russell reference is discloses a method and apparatus for

providing a dielectric layer having a low dielectric constant. Applicants submit that the Russell reference does not teach or suggest the problem of reducing lateral silicide growth.

Since the Kang reference, the Merrill reference, and the Russell reference taken as a whole are silent with respect to the problem solved by Applicants' invention, it is respectfully submitted that there is no teaching or suggestion to combine the references to arrive at Applicants' invention as required by 35 USC §103.

Even if combined, however, the combination of the Kang reference, the Merrill reference, and the Russell reference fails to teach or suggest the Applicants' claimed invention. The Kang reference, the Merrill reference, and the Russell reference taken singly, or in combination, fail to disclose or suggest forming trenches in the semiconductor substrate at the outer edges of an insulating sidewall spacer around the gate.

Accordingly, it is submitted that Claim 9 as currently amended is patentable over the Kang reference in view of the Merrill reference in further view of the Russell reference taken singly, or in combination.

Claim 9 also has been rejected under 35 U.S.C. 103(a) as being unpatentable over the Kang reference in view of the Merrill reference as applied to claim 6 and further in view of the Sekiguchi reference.

In reference to claim 9, claim 9 depends on claim 6 and includes all the limitations thereof. Accordingly, claim 9 is patentable for the reasons set forth above with respect to claim 6.

Additionally, the Sekiguchi reference is directed to a semiconductor device having a "gas-dielectric interconnect structure" and does not teach or suggest the problem solved by Applicants invention. Since the Kang reference, the Merrill reference, and the Sekiguchi reference taken as a whole do not teach or suggest the problem solved by Applicants' invention, it is respectfully submitted that there is no teaching or suggestion to combine the references to arrive at Applicants' invention as required by 35 USC §103.

Even if combined, however, the combination of the Kang reference, the Merrill reference, and the Sekiguchi reference fails to disclose or suggest the Applicants' claimed

invention. The Kang reference, the Merrill reference, and the Sekiguchi reference taken singly, or in combination, fail to disclose or suggest forming trenches in the semiconductor substrate at the outer edges of an insulating sidewall spacer around the gate.

Accordingly, it is submitted that Claim 9 as currently amended is patentable over the Kang reference in view of the Merrill reference in further view of the Sekiguchi reference taken singly, or in combination.

Claim 10 has been rejected under 35 U.S.C. 103(a) as being unpatentable over the Kang reference in view of Merrill reference as applied to claim 6 above and further in view of the Liauh reference and further in view of the Wald reference.

Applicants traverse this rejection. Claim 10 depends on claim 6 and includes all the limitations thereof. Accordingly, claim 10 is patentable for the reasons set forth above with respect to claim 6.

Additionally, in reference to claim 10, the Kang reference discloses a metal oxide semiconductor device in which an insulating sidewall spacer is removed to form a groove structure in the substrate adjacent the gate. A polysilicon layer is formed on the groove structure to form a second gate electrode at both sides of the gate (see col. 2, lines 48-56). There is no insulating sidewall spacer around the gate in the Kang reference as claimed by Applicants. The "sidewall spacer" referred to by the Examiner in the Kang reference is a second gate electrode not an "insulating sidewall spacer" as claimed by Applicant.

The Examiner has stated:

> Kang does not disclose the use of a silicide with the source/drain junctions ...

Applicants agree and submit that the Kang reference therefore cannot, and does not, recognize or address the problem solved by Applicants' invention. Since there is no silicide disclosed or suggested in the Kang reference, there can be no suggestion that the structure or method disclosed in the Kang reference recognizes or addresses reducing lateral silicide growth toward the channel of the transistor.

The Examiner also has stated:

> Kang does not disclose the exact material which is used for the contact.

Applicants agree that the Kang reference does not disclose the materials used for contacts as claimed by Applicants.

The Merrill reference is directed to a semiconductor device using a silicide to reduce contact resistance. The Merrill reference does not disclose or suggest the problem of lateral silicide growth or a proposed solution.

Since both the Kang reference and the Merrill reference are silent with respect to the problem solved by Applicants' invention, it is respectfully submitted that there is no teaching or suggestion to combine the references to arrive at Applicants' invention as required by 35 USC §103.

Even if combined, however, the combination of the Kang reference and the Merrill reference fails to disclose or suggest the Applicants' claimed invention. The Kang reference and the Merrill reference, taken either singly, or in combination, fail to disclose or suggest forming trenches in the semiconductor substrate at the outer edges of an insulating sidewall spacer around the gate. The Kang reference and the Merrill reference, taken either singly, or in combination, also fail to disclose or suggest the contact materials claimed by Applicants.

The Liauh reference is directed to a process for forming a polycide gate structure including a metal salicide to reduce sheet resistance of the gate, and having metal silicides formed in the source and drain regions to minimize sheet resistance. The Liauh reference does not disclose the problem of lateral silicide growth or any proposed solution.

Similarly, the Wald reference does not disclose the problem of lateral silicide growth or any proposed solution.

Since the Kang reference, the Merrill reference, the Liauh reference, and the Wald reference taken as a whole are silent with respect to the problem solved by Applicants' invention, it is respectfully submitted that there is no teaching or suggestion to combine these references to arrive at Applicants' invention as required by 35 USC §103.

Even if combined, however, the combination of the proposed combination of the Kang reference, the Merrill reference, the Liauh reference, and the Wald reference fails to disclose or suggest the Applicants' claimed invention. These references, taken either singly, or in combination, fail to disclose or suggest forming trenches in the semiconductor substrate at the outer edges of an insulating sidewall spacer around the gate.

Accordingly, it is submitted that Claim 9 as currently amended is patentable over the Kang reference in view of the Merrill reference in further view of the Liauh reference and in further view of the Wald reference taken singly, or in combination.

Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over the Kang reference in view of the Merrill reference as applied to claim 6 above and further in view of the Liauh reference and further in view of the Yoshida reference.

Applicants traverse this rejection. Claim 10 depends on claim 6 and includes all the limitations thereof. Accordingly, claim 10 is patentable for the reasons set forth above with respect to claim 6.

Additionally, in reference to claim 10, the Kang reference discloses a metal oxide semiconductor device in which an insulating sidewall spacer is removed to form a groove structure in the substrate adjacent the gate. A polysilicon layer is formed on the groove structure to form a second gate electrode at both sides of the gate (see col. 2, lines 48-56). There is no insulating sidewall spacer around the gate in the Kang reference as claimed by Applicants. The "sidewall spacer" referred to by the Examiner in the Kang reference is a second gate electrode not an "insulating sidewall spacer" as claimed by Applicant.

The Examiner has stated:

> Kang does not disclose the use of a silicide with the source/drain junctions ...

Applicants agree and submit that the Kang reference therefore cannot, and does not, recognize or address the problem solved by Applicants' invention. Since there is no silicide disclosed or suggested in the Kang reference, there can be no suggestion that the structure or method disclosed in the Kang reference recognizes or addresses reducing lateral silicide growth toward the channel of the transistor.

The Examiner also has stated:

> Kang does not disclose the exact material which is used for the contact.

Applicants agree that the Kang reference does not disclose the materials used for contacts as claimed by Applicants.

The Merrill reference is directed to a semiconductor device using a silicide to reduce contact resistance. The Merrill reference does not disclose or suggest the problem of lateral silicide growth or a proposed solution.

Since both the Kang reference and the Merrill reference taken as a whole are silent with respect to the problem solved by Applicants' invention, it is respectfully submitted that there is no teaching or suggestion to combine the references to arrive at Applicants' invention as required by 35 USC §103.

Even if combined, however, the combination of the Kang reference and the Merrill reference fails to disclose or suggest the Applicants' claimed invention. The Kang reference and the Merrill reference, taken either singly, or in combination, fail to disclose or suggest an integrated circuit including an insulating liner around the gate, an insulating film over the insulating liner, and trenches in the semiconductor substrate at the outer edges of the insulating film. The Kang reference and the Merrill reference, taken either singly, or in combination, also fail to disclose or suggest the contact materials claimed by Applicants.

The Liauh reference is directed to a process for forming a polycide gate structure including a metal salicide to reduce sheet resistance of the gate, and having metal silicides formed in the source and drain regions to minimize sheet resistance. The Liauh reference does not disclose the problem of lateral silicide growth or any proposed solution.

Similarly, the Yoshida reference does not disclose the problem of lateral silicide growth or any proposed solution. The Yoshida reference is directed to a thin-film circuit substrate having an organic insulating film with a surface modification layer.

Since the Kang reference, the Merrill reference, the Liauh reference, and the Yoshida reference taken as a whole are silent with respect to the problem solved by Applicants' invention, it is respectfully submitted that there is no teaching or suggestion to combine these references to arrive at Applicants' invention as required by 35 USC §103.

Even if combined, however, the proposed combination of the Kang reference, the Merrill reference, the Liauh reference, and the Yoshida reference fails to disclose or suggest the Applicants' claimed invention. These references, taken either singly, or in combination, fail to disclose or suggest an integrated circuit including an insulating liner around the gate,

an insulating film over the insulating liner, and trenches in the semiconductor substrate at the outer edges of the insulating film.

Accordingly, it is submitted that Claim 10 as currently amended is patentable over the Kang reference, the Merrill reference, the Liauh reference, and the Yoshida reference taken singly, or in combination.

Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over the Kang reference in view of the Merrill reference as applied to claim 11 above and further in view of the Russell reference.

Applicants traverse this rejection. In reference to claim 14, claim 14 depends on claim 11 and includes all the limitations thereof. Accordingly, claim 14 is patentable for the reasons set forth above with respect to claim 11.

Additionally, the Russell reference does not disclose or suggest the problem solved by Applicants' invention. The Russell reference is discloses a method and apparatus for providing a dielectric layer having a low dielectric constant. Applicants submit that the Russell reference does not disclose or suggest the problem of reducing lateral silicide growth.

Since the Kang reference, the Merrill reference, and the Russell reference are silent with respect to the problem solved by Applicants' invention, it is respectfully submitted that there is no teaching or suggestion to combine the references to arrive at Applicants' invention as required by 35 USC §103.

Even if combined, however, the combination of the Kang reference, the Merrill reference, and the Russell reference fails to disclose or suggest the Applicants' claimed invention. The Kang reference, the Merrill reference, and the Russell reference taken singly, or in combination, fail to disclose or suggest trenches in the source/drain junctions of the semiconductor substrate around the outer edge of the insulating spacer.

Accordingly, it is submitted that Claim 14 is patentable over the Kang reference in view of the Merrill reference in further view of the Russell reference taken singly, or in combination.

Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over the Kang reference in view of the Merrill reference as applied to claim 11 above and further in view of the Sekiguchi reference.

Applicants traverse this rejection. Claim 14 depends on claim 11 and includes all the limitations set forth therein. Accordingly, claim 14 is patentable for the reasons set forth above with respect to claim 11.

Additionally, the Sekiguchi reference is directed to a semiconductor device having a "gas-dielectric interconnect structure" and does not disclose or suggest the problem solved by Applicants invention. Since the Kang reference, the Merrill reference, and the Sekiguchi reference are silent with respect to the problem solved by Applicants' invention, it is respectfully submitted that there is no teaching or suggestion to combine the references to arrive at Applicants' invention as required by 35 USC §103.

Even if combined, however, the combination of the Kang reference, the Merrill reference, and the Sekiguchi reference fails to disclose or suggest the Applicants' claimed invention. The Kang reference, the Merrill reference, and the Sekiguchi reference taken singly, or in combination, fail to disclose or suggest trenches in the source/drain junctions of the semiconductor substrate around the outer edge of the insulating spacer.

Accordingly, it is submitted that Claim 14 is patentable over the Kang reference in view of the Merrill reference in further view of the Sekiguchi reference taken singly, or in combination.

Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over the Kang reference in view of the Merrill reference as applied to claim 11 above and further in view of the Liauh reference and further in view of the Wald reference.

Applicants traverse this rejection. Claim 15 depends on claim 11 as currently amended and includes the limitations set forth therein. Accordingly, claim 15 is patentable for the reasons set forth above with respect to claim 11.

In reference to claim 15, the Kang reference discloses a metal oxide semiconductor device in which an insulating sidewall spacer is removed to form a groove structure in the substrate adjacent the gate. A polysilicon layer is formed on the groove structure to form a

second gate electrode at both sides of the gate (see col. 2, lines 48-56). There is no insulating sidewall spacer around the gate in the Kang reference as claimed by Applicants. The "sidewall spacer" referred to by the Examiner in the Kang reference is a second gate electrode not an "insulating sidewall spacer" as claimed by Applicant.

The Examiner has stated:

> Kang does not disclose the use of a silicide with the source/drain junctions ...

Applicants agree and submit that the Kang reference therefore cannot, and does not, recognize or address the problem solved by Applicants' invention. Since there is no silicide disclosed or suggested in the Kang reference, there can be no suggestion that the structure or method disclosed in the Kang reference recognizes or addresses reducing lateral silicide growth toward the channel of the transistor.

The Examiner also has stated:

> Kang does not disclose the exact material which is used for the contact.

Applicants agree that the Kang reference does not disclose the materials used for contacts as claimed by Applicants.

The Merrill reference is directed to a semiconductor device using a silicide to reduce contact resistance. The Merrill reference does not disclose or suggest the problem of lateral silicide growth or a proposed solution.

Since both the Kang reference and the Merrill reference taken as a whole are silent with respect to the problem solved by Applicants' invention, it is respectfully submitted that there is no teaching or suggestion to combine the references to arrive at Applicants' invention as required by 35 USC §103.

Even if combined, however, the combination of the Kang reference and the Merrill reference fails to disclose or suggest the Applicants' claimed invention. The Kang reference and the Merrill reference, taken either singly, or in combination, fail to disclose or suggest forming trenches at the outer edges of an insulating spacer around the gate of a transistor. The Kang reference and the Merrill reference, taken either singly, or in combination, also fail to disclose or suggest the contact materials claimed by Applicants.

The Liauh reference is directed to a process for forming a polycide gate structure including a metal salicide to reduce sheet resistance of the gate, and having metal silicides formed in the source and drain regions to minimize sheet resistance. The Liauh reference does not disclose the problem of lateral silicide growth or any proposed solution.

Similarly, the Wald reference does not disclose the problem of lateral silicide growth or any proposed solution.

Since the Kang reference, the Merrill reference, the Liauh reference, and the Wald reference taken as a whole are silent with respect to the problem solved by Applicants' invention, it is respectfully submitted that there is no teaching or suggestion to combine these references to arrive at Applicants' invention as required by 35 USC §103.

Even if combined, however, the combination of the proposed combination of the Kang reference, the Merrill reference, the Liauh reference, and the Wald reference fails to disclose or suggest the Applicants' claimed invention. These references, taken either singly, or in combination, fail to disclose or suggest trenches in the source/drain junctions of the semiconductor substrate around the outer edge of the insulating spacer.

Accordingly, it is submitted that Claim 15 as currently amended is patentable over the Kang reference, the Merrill reference, the Liauh reference, and the Wald reference taken singly, or in combination.

Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over the Kang reference in view of the Merrill reference as applied to claim 11 above and further in view of the Liauh reference and further in view of the Yoshida reference.

Claim 15 depends on currently amended claim 11 and includes all the limitations thereof. Accordingly, claim 15 is patentable for the reasons set forth with regard to claim 11.

In reference to claim 15, the Kang reference discloses a metal oxide semiconductor device in which an insulating sidewall spacer is removed to form a groove structure in the substrate adjacent the gate. A polysilicon layer is formed on the groove structure to form a second gate electrode at both sides of the gate (see col. 2, lines 48-56). There is no insulating sidewall spacer around the gate in the Kang reference as claimed by Applicants. The

"sidewall spacer" referred to by the Examiner in the Kang reference is a second gate electrode not an "insulating sidewall spacer" as claimed by Applicant.

The Examiner has stated:

> Kang does not disclose the use of a silicide with the source/drain junctions ...

Applicants agree and submit that the Kang reference therefore cannot, and does not, recognize or address the problem solved by Applicants' invention. Since there is no silicide disclosed or suggested in the Kang reference, there can be no suggestion that the structure or method disclosed in the Kang reference recognizes or addresses reducing lateral silicide growth toward the channel of the transistor.

The Examiner also has stated:

> Kang does not disclose the exact material which is used for the contact.

Applicants agree that the Kang reference does not disclose the materials used for contacts as claimed by Applicants.

The Merrill reference is directed to a semiconductor device using a silicide to reduce contact resistance. The Merrill reference does not disclose or suggest the problem of lateral silicide growth or a proposed solution.

Since both the Kang reference and the Merrill reference taken as a whole are silent with respect to the problem solved by Applicants' invention, it is respectfully submitted that there is no teaching or suggestion to combine the references to arrive at Applicants' invention as required by 35 USC §103.

Even if combined, however, the combination of the Kang reference and the Merrill reference fails to disclose or suggest the Applicants' claimed invention. The Kang reference and the Merrill reference, taken either singly, or in combination, fail to disclose or suggest trenches in the source/drain junctions of the semiconductor substrate around the outer edge of the insulating spacer. The Kang reference and the Merrill reference, taken either singly, or in combination, also fail to disclose or suggest the contact materials claimed by Applicants.

The Liauh reference is directed to a process for forming a polycide gate structure including a metal salicide to reduce sheet resistance of the gate, and having metal silicides

formed in the source and drain regions to minimize sheet resistance. The Liauh reference does not disclose the problem of lateral silicide growth or any proposed solution.

Similarly, the Yoshida reference does not disclose the problem of lateral silicide growth or any proposed solution. The Yoshida reference is directed to a thin-film circuit substrate having an organic insulating film with a surface modification layer.

Since the Kang reference, the Merrill reference, the Liauh reference, and the Yoshida reference taken as a whole are silent with respect to the problem solved by Applicants' invention, it is respectfully submitted that there is no teaching or suggestion to combine these references to arrive at Applicants' invention as required by 35 USC §103.

Even if combined, however, the proposed combination of the Kang reference, the Merrill reference, the Liauh reference, and the Yoshida reference fails to disclose or suggest the Applicants' claimed invention. These references, taken either singly, or in combination, fail to disclose or suggest trenches in the source/drain junctions of the semiconductor substrate around the outer edge of the insulating spacer.

Accordingly, it is submitted that Claim 15 as currently amended is patentable over the Kang reference, the Merrill reference, the Liauh reference, and the Yoshida reference taken singly, or in combination. .

Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over the Kang reference in view of the Merrill reference as applied to claim 16 above and further in view of the Russell reference.

Applicants traverse this rejection. In reference to claim 19, claim 19 depends on claim 16 and includes all the limitations thereof. Accordingly, claim 19 is patentable for the reasons set forth above with respect to claim 16.

Additionally, the Russell reference does not disclose or suggest the problem solved by Applicants' invention. The Russell reference is discloses a method and apparatus for providing a dielectric layer having a low dielectric constant. Applicants submit that the Russell reference does not disclose or suggest the problem of reducing lateral silicide growth.

Since the Kang reference, the Merrill reference, and the Russell reference are silent with respect to the problem solved by Applicants' invention, it is respectfully submitted that there is no teaching or suggestion to combine the references to arrive at Applicants' invention as required by 35 USC §103.

Even if combined, however, the combination of the Kang reference, the Merrill reference, and the Russell reference fails to disclose or suggest the Applicants' claimed invention. The Kang reference, the Merrill reference, and the Russell reference taken singly, or in combination, fail to disclose or suggest an integrated circuit having an insulating liner around the gate, an insulating film over the insulating liner, and trenches in the semiconductor substrate at the outer edges of the insulating film.

Accordingly, it is submitted that Claim 19 is patentable over the Kang reference in view of the Merrill reference in further view of the Russell reference taken singly, or in combination.

Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over the Kang reference in view of the Merrill reference as applied to claim 16 above and further in view of the Sekiguchi reference.

Applicants traverse this rejection. Claim 19 depends on claim 16 and includes all the limitations set forth therein. Accordingly, claim 19 is patentable for the reasons set forth above with respect to claim 16.

Additionally, the Sekiguchi reference is directed to a semiconductor device having a "gas-dielectric interconnect structure" and does not disclose or suggest the problem solved by Applicants invention. Since the Kang reference, the Merrill reference, and the Sekiguchi reference are silent with respect to the problem solved by Applicants' invention, it is respectfully submitted that there is no teaching or suggestion to combine the references to arrive at Applicants' invention as required by 35 USC §103.

Even if combined, however, the combination of the Kang reference, the Merrill reference, and the Sekiguchi reference fails to disclose or suggest the Applicants' claimed invention. The Kang reference, the Merrill reference, and the Sekiguchi reference taken singly, or in combination, fail to disclose or suggest an integrated circuit having an insulating

liner around the gate, an insulating film over the insulating liner, and trenches in the semiconductor substrate at the outer edges of the insulating film.

Accordingly, it is submitted that Claim 19 is patentable over the Kang reference in view of the Merrill reference in further view of the Russell reference taken singly, or in combination.

Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over the Kang reference in view of the Merrill reference as applied to claim 16 above and further in view of the Liauh reference and further in view of the Wald reference.

Applicants traverse this rejection. Claim 20 depends on claim 16 as currently amended and includes the limitations set forth therein. Accordingly, claim 20 is patentable for the reasons set forth above with respect to claim 16.

In reference to claim 20, the Kang reference discloses a metal oxide semiconductor device in which an insulating sidewall spacer is removed to form a groove structure in the substrate adjacent the gate. A polysilicon layer is formed on the groove structure to form a second gate electrode at both sides of the gate (see col. 2, lines 48-56). There is no insulating sidewall spacer around the gate in the Kang reference as claimed by Applicants. The "sidewall spacer" referred to by the Examiner in the Kang reference is a second gate electrode not an "insulating sidewall spacer" as claimed by Applicant.

The Examiner has stated:

> Kang does not disclose the use of a silicide with the source/drain junctions ...

Applicants agree and submit that the Kang reference therefore cannot, and does not, recognize or address the problem solved by Applicants' invention. Since there is no silicide disclosed or suggested in the Kang reference, there can be no suggestion that the structure or method disclosed in the Kang reference recognizes or addresses reducing lateral silicide growth toward the channel of the transistor.

The Examiner also has stated:

> Kang does not disclose the exact material which is used for the contact.

Applicants agree that the Kang reference does not disclose the materials used for contacts as claimed by Applicants.

The Merrill reference is directed to a semiconductor device using a silicide to reduce contact resistance. The Merrill reference does not disclose or suggest the problem of lateral silicide growth or a proposed solution.

Since both the Kang reference and the Merrill reference taken as a whole are silent with respect to the problem solved by Applicants' invention, it is respectfully submitted that there is no teaching or suggestion to combine the references to arrive at Applicants' invention as required by 35 USC §103.

Even if combined, however, the combination of the Kang reference and the Merrill reference fails to disclose or suggest the Applicants' claimed invention. The Kang reference and the Merrill reference, taken either singly, or in combination, fail to disclose or suggest an integrated circuit having an insulating liner around the gate, an insulating film over the insulating liner, and trenches in the semiconductor substrate at the outer edges of the insulating film. The Kang reference and the Merrill reference, taken either singly, or in combination, also fail to disclose or suggest the contact materials claimed by Applicants.

The Liauh reference is directed to a process for forming a polycide gate structure including a metal salicide to reduce sheet resistance of the gate, and having metal silicides formed in the source and drain regions to minimize sheet resistance. The Liauh reference does not disclose the problem of lateral silicide growth or any proposed solution.

Similarly, the Wald reference does not disclose the problem of lateral silicide growth or any proposed solution.

Since the Kang reference, the Merrill reference, the Liauh reference, and the Wald reference are silent with respect to the problem solved by Applicants' invention, it is respectfully submitted that there is no teaching or suggestion to combine these references to arrive at Applicants' invention as required by 35 USC §103.

Even if combined, however, the combination of the proposed combination of the Kang reference, the Merrill reference, the Liauh reference, and the Wald reference fails to disclose or suggest the Applicants' claimed invention. These references, taken either singly, or in combination, fail to disclose or suggest an integrated circuit having an insulating liner around

the gate, an insulating film over the insulating liner, and trenches in the semiconductor substrate at the outer edges of the insulating film.

Accordingly, it is submitted that Claim 20 as currently amended is patentable over the Kang reference, the Merrill reference, the Liauh reference, and the Wald reference taken singly, or in combination.

Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over the Kang reference in view of the Merrill reference as applied to claim 16 above and further in view of the Liauh reference and further in view of the Yoshida reference.

Claim 20 depends on currently amended claim 16 and includes all the limitations thereof. Accordingly, claim 20 is patentable for the reasons set forth with regard to claim 16.

In reference to claim 20, the Kang reference discloses a metal oxide semiconductor device in which an insulating sidewall spacer is removed to form a groove structure in the substrate adjacent the gate. A polysilicon layer is formed on the groove structure to form a second gate electrode at both sides of the gate (see col. 2, lines 48-56). There is no insulating sidewall spacer around the gate in the Kang reference as claimed by Applicants. The "sidewall spacer" referred to by the Examiner in the Kang reference is a second gate electrode not an "insulating sidewall spacer" as claimed by Applicant.

The Examiner has stated:

> Kang does not disclose the use of a silicide with the source/drain junctions ...

Applicants agree and submit that the Kang reference therefore cannot, and does not, recognize or address the problem solved by Applicants' invention. Since there is no silicide disclosed or suggested in the Kang reference, there can be no suggestion that the structure or method disclosed in the Kang reference recognizes or addresses reducing lateral silicide growth toward the channel of the transistor.

The Examiner also has stated:

> Kang does not disclose the exact material which is used for the contact.

Applicants agree that the Kang reference does not disclose the materials used for contacts as claimed by Applicants.

The Merrill reference is directed to a semiconductor device using a silicide to reduce contact resistance. The Merrill reference does not disclose or suggest the problem of lateral silicide growth or a proposed solution.

Since both the Kang reference and the Merrill reference taken as a whole are silent with respect to the problem solved by Applicants' invention, it is respectfully submitted that there is no teaching or suggestion to combine the references to arrive at Applicants' invention as required by 35 USC §103.

Even if combined, however, the combination of the Kang reference and the Merrill reference fails to disclose or suggest the Applicants' claimed invention. The Kang reference and the Merrill reference, taken either singly, or in combination, fail to disclose or suggest an integrated circuit having an insulating liner around the gate, an insulating film over the insulating liner, and trenches in the semiconductor substrate at the outer edges of the insulating film. The Kang reference and the Merrill reference, taken either singly, or in combination, also fail to disclose or suggest the contact materials claimed by Applicants.

The Liauh reference is directed to a process for forming a polycide gate structure including a metal salicide to reduce sheet resistance of the gate, and having metal silicides formed in the source and drain regions to minimize sheet resistance. The Liauh reference does not disclose the problem of lateral silicide growth or any proposed solution.

Similarly, the Yoshida reference does not disclose the problem of lateral silicide growth or any proposed solution. The Yoshida reference is directed to a thin-film circuit substrate having an organic insulating film with a surface modification layer.

Since the Kang reference, the Merrill reference, the Liauh reference, and the Yoshida reference taken as a whole are silent with respect to the problem solved by Applicants' invention, it is respectfully submitted that there is no teaching or suggestion to combine these references to arrive at Applicants' invention as required by 35 USC §103.

Even if combined, however, the proposed combination of the Kang reference, the Merrill reference, the Liauh reference, and the Yoshida reference fails to disclose or suggest the Applicants' claimed invention. These references, taken either singly, or in combination, fail to disclose or suggest an integrated circuit having an insulating liner around the gate, an

insulating film over the insulating liner, and trenches in the semiconductor substrate at the outer edges of the insulating film.

Accordingly, it is submitted that Claim 20 as currently amended is patentable over the Kang reference, the Merrill reference, the Liauh reference, and the Yoshida reference taken singly, or in combination.

Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over the Iinuma reference in view of the Russell reference.

Applicants respectfully traverse this rejection since the Applicants' claimed combination, as exemplified in claim 1, includes the limitation not disclosed in the Iinuma reference of forming trenches in the semiconductor substrate around the gate. Claim 1 has now been amended to clarify the invention and not for reasons related to patentability. The previously claimed combination, as exemplified in claim 1, has been amended to set forth more clearly that the sidewall spacer is an insulating sidewall spacer and that the trenches are formed in the source/drain junctions in the semiconductor substrate at the outer edge of the insulating sidewall spacer.

The Iinuma reference discloses a semiconductor device including an element separating insulating film to separate an element region. A silicide film over the source drain regions extends onto the element separating insulating film. A contact hole extends through an interlayer insulating film, the element separating film, and reaches the silicide film. The contact hole includes a trench portion whose one end contacts the edge of the silicide film in the bottom of the contact hole and in an upper portion of the element separating insulating film. The trench in the Iinuma reference is formed in the element separating insulating film in the bottom of the contact holes and not at the outer edge of an insulating sidewall spacer as claimed by Applicants.

Additionally, the Iinuma reference specifically discloses that it is possible to prevent the trench portion from contacting the first diffusion region, or source drain region (see col.7, l. 48-50). It is clear from Applicants' disclosure that the trenches in the present invention do contact the source/drain regions, therefore the Iinuma reference teaches away from Applicants' invention.

Furthermore, the Iinuma reference does not disclose or suggest the problem solved by Applicants' invention, i.e. reducing lateral silicide growth into the channel of the transistor, much less solve it. The Iinuma reference is directed to an entirely different problem of formation of an abnormally grown silicide film at the outer edges of the source/drain regions (see col. 7, l. 52-53 and FIG. 13, element 142).

In reference to claim 1 from the above, it is evident that the Iinuma reference lacks forming trenches around the gate at the outer edges of an insulating spacer as exemplified in currently amended claim 1. In light of the foregoing, applicants submit that claim 1, as amended, is patentable over the Iinuma reference.

Claim 4 depends on claim 1 and includes the limitations set forth therein. Accordingly, claim 4 is patentable for the reasons set forth above with respect to claim 1.

Additionally, the Russell reference does not disclose or suggest the problem solved by Applicants' invention. The Russell reference discloses a method and apparatus for providing a dielectric layer having a low dielectric constant. Applicants submit that the Russell reference does not disclose or suggest the problem of reducing lateral silicide growth.

Since the Iinuma reference and the Russell reference are silent with respect to the problem solved by Applicants' invention, it is respectfully submitted that there is no teaching or suggestion to combine the references to arrive at Applicants' invention as required by 35 USC §103.

Even if combined, however, the combination of the Iinuma reference and the Russell reference fails to disclose or suggest the Applicants' claimed invention. The Iinuma reference and the Russell reference taken singly, or in combination, fail to disclose or suggest forming trenches at the outer edges of an insulating spacer around the gate of a transistor.

Accordingly, it is submitted that Claim 4 is patentable over the Iinuma reference in view of the Russell reference taken singly, or in combination.

Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over the Iinuma reference in view of the Sekiguchi reference.

Applicants respectfully traverse this rejection since the Applicants' claimed combination, as exemplified in claim 1, includes the limitation not disclosed in the Iinuma reference of forming trenches in the semiconductor substrate around the gate. Claim 1 has now been amended to clarify the invention and not for reasons related to patentability. The previously claimed combination, as exemplified in claim 1, has been amended to set forth more clearly that the sidewall spacer is an insulating sidewall spacer and that the trenches are formed in the source/drain junctions in the semiconductor substrate at the outer edge of the insulating sidewall spacer.

The Iinuma reference discloses a semiconductor device including an element separating insulating film to separate an element region. A silicide film over the source drain regions extends onto the element separating insulating film. A contact hole extends through an interlayer insulating film, the element separating film, and reaches the silicide film. The contact hole includes a trench portion whose one end contacts the edge of the silicide film in the bottom of the contact hole and in an upper portion of the element separating insulating film. The trench in the Iinuma reference is formed in the element separating insulating film in the bottom of the contact holes and not at the outer edge of an insulating sidewall spacer as claimed by Applicants.

Additionally, the Iinuma reference specifically discloses that it is possible to prevent the trench portion from contacting the first diffusion region, or source drain region (see col.7, l. 48-50). It is clear from Applicants' disclosure that the trenches in the present invention do contact the source/drain regions, therefore the Iinuma reference teaches away from Applicants' invention.

Furthermore, the Iinuma reference does not disclose or suggest the problem solved by Applicants' invention, i.e. reducing lateral silicide growth into the channel of the transistor, much less solve it. The Iinuma reference is directed to an entirely different problem of formation of an abnormally grown silicide film at the outer edges of the source/drain regions (see col. 7, l. 52-53 and FIG. 13, element 142).

In reference to claims 1 from the above, it is evident that the Iinuma reference lacks forming trenches around the gate at the outer edges of an insulating spacer as exemplified in currently amended claim 1. In light of the foregoing, applicants submit that claim 1, as amended, is patentable over the Iinuma reference.

Claim 4 depends on claim 1 and includes the limitations set forth therein. Accordingly, claim 4 is patentable for the reasons set forth above with respect to claim 1.

Additionally, the Sekiguchi reference is directed to a semiconductor device having a "gas-dielectric interconnect structure" and does not disclose or suggest the problem solved by Applicants invention. Since the Iinuma reference and the Sekiguchi reference are silent with respect to the problem solved by Applicants' invention, it is respectfully submitted that there is no teaching or suggestion to combine the references to arrive at Applicants' invention as required by 35 USC §103.

Even if combined, however, the combination of the Iinuma reference and the Sekiguchi reference fails to disclose or suggest the Applicants' claimed invention. The Iinuma reference and the Sekiguchi reference taken singly, or in combination, fail to disclose or suggest forming trenches at the outer edges of an insulating spacer around the gate of a transistor.

Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over the Iinuma reference in view of the Russell reference.

Applicants respectfully traverse this rejection since the Applicants' claimed combination, as exemplified in claim 11, includes the limitation not disclosed in the Iinuma reference of forming trenches in the semiconductor substrate around the gate. Claim 11 has now been amended to clarify the invention, and not for reasons related to patentability. The previously claimed combination, as exemplified in claim 11, has been amended to set forth more clearly that the sidewall spacer is an insulating sidewall spacer and that the trenches are formed in the source/drain junctions in the semiconductor substrate at the outer edge of the insulating sidewall spacer.

The Iinuma reference discloses a semiconductor device including an element separating insulating film to separate an element region. A silicide film over the source drain

regions extends onto the element separating insulating film. A contact hole extends through an interlayer insulating film, the element separating film, and reaches the silicide film. The contact hole includes a trench portion whose one end contacts the edge of the silicide film in the bottom of the contact hole and in an upper portion of the element separating insulating film. The trench in the Iinuma reference is formed in the element separating insulating film in the bottom of the contact holes and not at the outer edge of an insulating sidewall spacer as claimed by Applicants.

Additionally, the Iinuma reference specifically discloses that it is possible to prevent the trench portion from contacting the first diffusion region, or source drain region (see col.7, l. 48-50). It is clear from Applicants' disclosure that the trenches in the present invention do contact the source/drain regions, therefore the Iinuma reference teaches away from Applicants' invention.

Furthermore, the Iinuma reference does not disclose or suggest the problem solved by Applicants' invention, i.e. reducing lateral silicide growth into the channel of the transistor, much less solve it. The Iinuma reference is directed to an entirely different problem of formation of an abnormally grown silicide film at the outer edges of the source/drain regions (see col. 7, l. 52-53 and FIG. 13, element 142).

In reference to claim 11 from the above, it is evident that the Iinuma reference lacks forming trenches around the gate at the outer edges of an insulating spacer as exemplified in currently amended claim 11. In light of the foregoing, applicants submit that claim 11, as amended, is patentable over the Iinuma reference.

Claim 14 depends on claim 11 and includes the limitations set forth therein. Accordingly, claim 14 is patentable for the reasons set forth above with respect to claim 11.

Additionally, the Russell reference does not disclose or suggest the problem solved by Applicants' invention. The Russell reference discloses a method and apparatus for providing a dielectric layer having a low dielectric constant. Applicants submit that the Russell reference does not disclose or suggest the problem of reducing lateral silicide growth.

Since the Iinuma reference and the Russell reference taken as a whole are silent with respect to the problem solved by Applicants' invention, it is respectfully submitted that there

is no teaching or suggestion to combine the references to arrive at Applicants' invention as required by 35 USC §103.

Even if combined, however, the combination of the Iinuma reference and the Russell reference fails to disclose or suggest the Applicants' claimed invention. The Iinuma reference and the Russell reference taken singly, or in combination, fail to disclose or suggest trenches at the outer edges of an insulating spacer around the gate of a transistor.

Accordingly, it is submitted that Claim 14 is patentable over the Iinuma reference in view of the Russell reference taken singly, or in combination.

Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over the Iinuma reference in view of the Sekiguchi reference.

Applicants respectfully traverse this rejection since the Applicants' claimed combination, as exemplified in claim 11, includes the limitation not disclosed in the Iinuma reference of forming trenches in the semiconductor substrate around the gate. Claim 11 has now been amended to clarify the invention and not for reasons related to patentability. The previously claimed combination, as exemplified in claim 11, has been amended to set forth more clearly that the sidewall spacer is an insulating sidewall spacer and that the trenches are formed in the source/drain junctions in the semiconductor substrate at the outer edge of the insulating sidewall spacer.

The Iinuma reference discloses a semiconductor device including an element separating insulating film to separate an element region. A silicide film over the source drain regions extends onto the element separating insulating film. A contact hole extends through an interlayer insulating film, the element separating film, and reaches the silicide film. The contact hole includes a trench portion whose one end contacts the edge of the silicide film in the bottom of the contact hole and in an upper portion of the element separating insulating film. The trench in the Iinuma reference is formed in the element separating insulating film in the bottom of the contact holes and not at the outer edge of an insulating sidewall spacer as claimed by Applicants.

Additionally, the Iinuma reference specifically discloses that it is possible to prevent the trench portion from contacting the first diffusion region, or source drain region (see col.7,

l. 48-50). It is clear from Applicants' disclosure that the trenches in the present invention do contact the source/drain regions, therefore the Iinuma reference teaches away from Applicants' invention.

Furthermore, the Iinuma reference does not disclose or suggest the problem solved by Applicants' invention, i.e. reducing lateral silicide growth into the channel of the transistor, much less solve it. The Iinuma reference is directed to an entirely different problem of formation of an abnormally grown silicide film at the outer edges of the source/drain regions (see col. 7, l. 52-53 and FIG. 13, element 142).

In reference to claim 11 from the above, it is evident that the Iinuma reference lacks trenches around the gate at the outer edges of an insulating spacer as exemplified in currently amended claim 11. In light of the foregoing, applicants submit that claim 11, as amended, is patentable over the Iinuma reference.

Claim 14 depends on claim 11 and includes the limitations set forth therein. Accordingly, claim 14 is patentable for the reasons set forth above with respect to claim 11.

Additionally, the Sekiguchi reference is directed to a semiconductor device having a "gas-dielectric interconnect structure" and does not disclose or suggest the problem solved by Applicants invention. Since the Iinuma reference and the Sekiguchi reference are silent with respect to the problem solved by Applicants' invention, it is respectfully submitted that there is no teaching or suggestion to combine the references to arrive at Applicants' invention as required by 35 USC §103.

Even if combined, however, the combination of the Iinuma reference and the Sekiguchi reference fails to disclose or suggest the Applicants' claimed invention. The Iinuma reference and the Sekiguchi reference taken singly, or in combination, fail to disclose or suggest trenches at the outer edges of an insulating spacer around the gate of a transistor.

Accordingly, it is submitted that Claim 14 is patentable over the Iinuma reference in view of the Sekiguchi reference taken singly or in combination.

Double Patenting

The Examiner has stated that should claim 3 be found allowable, claim 8 will be objected to under 37 CFR 1.75 as being a substantial duplicate thereof, and that should claim 4 be found allowable, claim 9 will be objected to under 37 CFR 1.75 as being a substantial duplicate thereof.

Applicants have amended claims 8 and 9 to correct typographical errors so that claims 8 and 9 now depend from claim 6 rather than claim 1. Accordingly, it is respectfully submitted that the advisory double patenting objection is no longer proper and should be withdrawn.

Conclusion

In view of the above, it is submitted that the claims are in condition for allowance and reconsideration of the rejections is respectfully requested. Allowance of claims 1, 3-16, and 18-24 at an early date is solicited.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including any extension of time fees, to Deposit Account No. 01-0365 and please credit any excess fees to such deposit account.

Respectfully submitted,

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